

REMARKS

Claim 1 has been amended to better define the claimed invention and better distinguish the claimed invention from the prior art.

The rejection of claims 1-6, 8-9 and 12-13 under 35 U.S.C. §102(e) as being anticipated by US Patent No. 6,541,840 to Terayama et al., the rejection of and claim 11 under 35 U.S.C. 103(a) as being unpatentable over Terayama et al. in view of U.S. Patent No. 6,768,171 to Disney, and the rejection of claims 7 and 10 as being unpatentable over Terayama et al. in view of U.S. Patent No. 6,259,136 to Kawaguchi are in error.

In rejecting the claims, the Examiner has taken issue with Applicants' previous arguments regarding the position of the first conductivity type semiconductor substrate relative to the second conductivity type semiconductor substrate (Office Action at page 7). Claim 1 calls for the second conductivity type semiconductor substrate to be *on* the first conductivity type semiconductor substrate. However, as noted in Amendment C, which is incorporated by reference, Terayama et al. does not teach this feature. Terayama et al. only teaches a capacitor formed between a device forming a portion and a second semiconductor layer. Notwithstanding the foregoing, to better distinguish claim 1 from the prior art, claim 1 has been amended to specify, in part:

“a device forming portion includes a first conductivity type well region and a second conductivity type well region” and

“said firsts conductivity type well region and said second conductivity type well region are provided on said top surface of said second conductivity type semiconductor layer.”

Thus, claim 1, as amended, requires “the second conductivity type semiconductor layer” is formed under the both of “the first conductivity type well region” and ”the second conductivity

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type well region" and a decoupling capacitor can be formed between "the second conductivity type well region" and "the first conductivity type semiconductor substrate". Accordingly, the capacitors can be formed under the both of "the first conductivity type well region" and "the second conductivity type well region".

Therefore, the capacitor of the present invention has a large area of the capacitance and the high capacitance value, compared to the capacitance of the reference Terayama et al. which has a capacitance only under the well region of either of the conductivity types.

Claim 8 further provides perspective, as previously claimed, requiring both the second conductivity type semiconductor substrate and a device forming portion being located on a top surface of the first conductivity type semiconductor substrate. The Examiner rejected this claim based on Terayama et al. by twisting FIG. 8(b) while reading claim 8. FIG. 8(b) does not feature a device forming portion on the same side of the first conductivity type semiconductor substrate as the second conductivity type semiconductor substrate. While the "top surface" of the first conductivity type semiconductor substrate may be relative, that term is not fluid within the claim.

Thus, claim 1 and claims 2-6, 8, 9, 12 and 13 which depend directly or indirectly on claim 1 cannot be said to be anticipated by Terayama et al.

Turning to the rejection of claim 11 as obvious from Terayama et al. in view of Disney, and claims 7 and 10 as obvious from Terayama et al. in view of Kawaguchi et al., it is submitted either secondary reference teaches or suggests the above discussed limitations of the claims that are missing from the teachings of Terayama, et al. Therefore, the Applicants respectfully request the allowance of claims 1 and all the claims that depend directly or indirectly thereon.

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Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action is respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on
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